CLAIMS

What is claimed is:

1. A semiconductor structure comprising:
an emitter mesa;
a base layer;
an emitter ledge layer located above the base layer and below the emitter mesa, the emitter ledge layer having an intrinsic region located beneath the emitter mesa and an extrinsic region located outside the intrinsic region, the extrinsic region comprising depleted semiconductor material; and
one or more base contacts formed within a portion of the extrinsic region of the emitter ledge layer and spaced at selected distances from the emitter mesa, wherein the one or more base contacts electrically contact the base layer, and
wherein the base contacts and the emitter ledge layer are disposed to cover an upper surface of the base layer so that there are no gaps in the emitter ledge layer between the one or more base contacts and the emitter mesa to leave the upper surface of the base layer exposed.

2. The semiconductor structure of claim 1, wherein the extrinsic region of the emitter ledge layer comprises fully depleted semiconductor material.

3. The semiconductor structure of claim 1, wherein the semiconductor structure comprises a portion of a heterojunction bipolar transistor (HBT).

4. The semiconductor structure of claim 3, wherein the HBT comprises an InP-based NPN HBT.

5. The semiconductor structure of claim 4, wherein the emitter mesa comprises:
an emitter cap layer comprising layers of n^+ InGaAs and n^+ AlInAs, and
an emitter layer comprising n^- AlInAs.

6. The semiconductor structure of claim 4, wherein the emitter mesa comprises:
an emitter cap layer comprising layers of n^+ InGaAs and n^+ InP;
an emitter layer comprising n^- InP; and,
an etch stop layer comprising AlGaInAs.

7. The semiconductor structure of claim 4, wherein the InP-based HBT comprises a single heterojunction bipolar transistor or a double heterojunction bipolar transistor.

8. The semiconductor structure of claim 1, wherein the emitter mesa is formed by etching down to the emitter ledge layer after an emitter contact is formed on the emitter mesa.

9. The semiconductor structure of claim 8, wherein one or more portions of the extrinsic region of the emitter ledge layer are etched down to the base region to open one or more areas for the one or more base contacts and the one or more base contacts are formed by depositing metal in the one or more areas.

10. The semiconductor structure of claim 9, wherein the one or more base contacts further comprise metal deposited on top of one or more portions of the emitter ledge layer, said metal deposited on top of the one or more portions of the emitter ledge layer in electrical contact with the metal deposited in the one or more areas.

11. The semiconductor structure of claim 1, wherein the extrinsic region of the emitter edge layer serves as a surface passivation layer for an upper surface of the base layer.

12. The semiconductor structure of claim 1, wherein the emitter ledge layer comprises n^- InP.

13. A method for fabricating a heterojunction bipolar transistor (HBT), comprising:
providing a substrate;
forming a collector layer and a base layer for the HBT on the substrate;
forming an emitter ledge layer above the base layer;
forming an emitter mesa region above the emitter ledge layer; and
forming one or more base contacts in the emitter ledge layer at selected distances from the emitter mesa, the one or more base contacts in electrical contact with the base layer,
wherein the emitter ledge layer has an intrinsic region located beneath the emitter mesa and an extrinsic region located outside the intrinsic region and the extrinsic region comprises depleted semiconductor material and wherein the one or more base contacts are formed in the extrinsic region and one or more base contacts and the emitter ledge layer are formed so that there are no gaps in the extrinsic region of the emitter ledge layer between the one or more base contacts and the emitter mesa to leave an upper surface of the base layer exposed.

14. The method of clam 13, wherein the extrinsic region comprises fully depleted semiconductor material.

15. The method of claim 13, wherein the HBT comprises an InP-based NPN HBT.

16. The method of claim 15, wherein the emitter mesa comprises:
an emitter cap layer comprising layers of n^+ InGaAs and n^+ AlInAs, and
an emitter layer comprising n^- AlInAs.

17. The method of claim 15, wherein the emitter mesa comprises:
an emitter cap layer comprising layers of n^+ InGaAs and n^+ InP;
an emitter layer comprising n^- InP; and
an etch stop layer comprising AlGaInAs.

18. The method of claim 15, wherein the InP-based HBT comprises a single heterojunction bipolar transistor or a double heterojunction bipolar transistor.

19. The method of claim 13, wherein the emitter mesa is formed by etching down to the emitter ledge layer after an emitter contact is formed.

20. The method of claim 19, further comprising:
applying a first patterned photoresist after the emitter mesa is formed and
using said first patterned photoresist mask to etch one or more portions of the extrinsic region of the emitter ledge layer down to the base layer to open one or more areas for the one or more base contacts.

21. The method of claim 20, further comprising forming base contacts by depositing metal in the one or more areas.

22. The method of claim 21, further comprising applying a second patterned photoresist to expose one or more areas for one or more expanded base contacts.

23. The method of claim 22, further comprising forming the one or more expanded base contacts by depositing metal in the exposed one or more areas.

24. The method of claim 13, wherein the extrinsic region of the emitter ledge layer serves as a surface passivation layer for an upper surface of the base layer.

25. The method of claim 13, wherein the emitter ledge layer comprises n^- InP.

26. A semiconductor structure comprising an InP-based NPN heterojunction bipolar transistor (HBT) wherein the InP-based NPN HBT has a fully depleted emitter ledge layer region disposed between one or more base contacts and an emitter mesa to 100% or nearly 100% passivate an upper surface of a base layer of the InP-based NPN HBT.

27. The semiconductor structure of claim 26, wherein the fully depleted emitter ledge layer region has no gaps in the emitter ledge layer between the one or more base contacts and the emitter mesa to leave an upper surface of the base layer exposed.